SAULT COLLEGE OF APPLIED ARTS & TECHNOLOGY

SAULT STE. MARIE, ONTARIO

COURSE OUTLINE

COURSE TITLE:	INTERFACING
CODE NO.:	CET 315 - 6
PROGRAM:	ELECTRICAL & ELECTRONIC
	X TECHNICIAN / TECHNOLOGIST
SEMESTER:	FIVE
AUTHOR:	PETER SAVICH
DATE:	AUGUST 13, 1991
PREVIOUS OUTLINE DATED:	AUGUST 13, 1990

APPROVED: _____ _____

DEAN DATE

COURSE NAME: **CODE NO.:**

INTERFACING CET 315 - 6

TOTAL CREDIT HOURS: 90

LENGTH OF COURSE: 6 HOURS PER WEEK FOR 16 WEEKS
THREE 1 HOUR THEORY CLASSES PER WEEK
ONE 3 HOUR LAB CLASS PER WEEK

PREREQUISITE(S): CET 228

I. PHILOSOPHY / GOALS

THE OBJECTIVE OF THIS COURSE IS TO ENHANCE THE STUDENT'S KNOWLEDGE OF MICROPROCESSOR THEORY, PRACTICE AND APPLICATIONS.
THE COURSE USES THE 8088 ASSEMBLY LANGUAGE TO PROVIDE THIS KNOWLEDGE OF MICROPROCESSORS. THE CET228 COURSE OFFERING IN FOURTH SEMESTER INTRODUCED HARDWARE INTERFACING AND INTERRUPTS. THE STUDENT OF THE CET315 COURSE WILL BE GIVEN TIME TO ACQUIRE THE INTERFACING SKILLS FOR SUCH PERIPHERAL DEVICES AS: KEYBOARDS, CONSOLES, DISK DRIVES. THE SUPPORT CHIPS SUCH AS: THE DMA CONTROLLER, RAM, ROM, PROGRAMMABLE PERIPHERAL INTERFACE (PPI), PROGRAMMABLE INTERRUPT CONTROLLER (PIC), AND THE PROGRAMMABLE INTERVAL TIMER (PIT), WILL ALL BE INTERFACED. THE MAT TRAINERS WILL BE USED TO EXPEDITE THE LABS.

THE PRINCIPAL OF OPERATION FOR THE PERIPHERALS SUCH AS DISK DRIVES, CONSOLES, KEYBOARDS IS THE SAME FOR A 8088 BASED MPU COMPUTER SYSTEM AS FOR A 68000 BASED MPU COMPUTER SYSTEM. STUDENTS ARE EXPECTED TO BE ABLE TO TAKE A COMPUTER SYSTEM AND ILLUSTRATE THE INTERACTION BETWEEN THE COMPONENTS AND THE SUBSYSTEM. SPECIFICALLY, THE TYPES OF MEMORY, BUS CONCEPTS, I/O SERVICING SHOULD BE ABLE TO BE DESCRIBED FOR BOTH MPU'S.

THE COURSE WILL INTRODUCE THE 68000 MPU AND ITS ASSEMBLY LANGUAGE. THE STUDENT WILL BE PROVIDED TIME TO ACQUIRE SKILLS IN EDITING, ASSEMBLING, LINKING, DEBUGGING SKILLS FOR RUNNING ASSEMBLY PROGRAMS. AS WITH THE 8088 MPU, THIS REQUIRES THE STUDENT TO FIRST UNDERSTAND THE REGISTERS, VARIOUS ADDRESSING MODES AND INSTRUCTION SETS AVAILABLE FOR THE 68000 MPU.

COURSE NAME: CODE NO.:

INTERFACING CET 315 - 6

II. STUDENT PERFORMANCE OBJECTIVES

UPON SUCCESSFUL COMPLETION OF THIS COURSE, THE STUDENT WILL BE ABLE TO:

1. USE THE MAT TRAINERS TO INTERFACE THE HARDWARE ASSOCIATED WITH MICROCOMPUTER SYSTEMS.

2. USE "DEBUG" TO SAVE, RETRIEVE, ASSEMBLE, UNASSEMBLE, TRACE, AND EXAMINE SIMPLE ASSEMBLY PROGRAMS.

3. DEMONSTRATE KNOWLEDGE OF THE 68000 MPU REGISTERS, ADDRESSING MODES, INSTRUCTION SET, BY CORRECTING AND IMPROVING ASSEMBLY LANGUAGE PROGRAMS PRESENTED TO HIM/HER.

4. TROUBLESHOOT MICROCOMPUTER SYSTEMS USING TECHNIQUES SUCH AS THE USE OF THE LOGIC ANALYZERS.

COURSE NAME: **CODE NO.:**

INTERFACING CET 315 - 6

III. TOPICS TO BE COVERED

1. ARCHITECTURE OF THE 8086/8088. X
2. MEMORY INTERFACE OF THE 8086/8088 X
3. MEMORY MAPPING FOR THE 8086/8088 AND THE SUPPORT CHIPS: PPI, PIT, PIC, DMA X
4. INPUT/OUTPUT INTERFACE OF THE 8086/8088 X
5. INTERRUPT INTERFACE OF THE 8086/8088
6. CONSOLES, KEYBOARDS, DISK DRIVES
7. REGISTERS, ADDRESSING MODES, AND INSTRUCTION SET OF THE 68000
8. ASYNCHRONOUS MEMORY AND I/O INTERFACE OF THE 68000
9. SYNCHRONOUS MEMORY AND I/O INTERFACE OF THE 68000
10. EXCEPTION PROCESSING OF THE 68000

COURSE NAME: CODE NO.:

INTERFACING CET 315 - 6

IV. LEARNING ACTIVITIES

LEARNING ACTIVITIES	REQUIRED RESOURCES
1.0 ARCHITECTURE OF THE 8088	
UPON SUCCESSFUL COMPLETION OF THIS REVIEW UNIT, THE STUDENT WILL BE ABLE TO:	TEXT:
1.1 DESCRIBE THE ARCHITECTURE OF THE 8088 BY LISTING THE: REGISTERS, ADDRESSING MODES, AND INSTRUCTION SET.	X
1.2 USING PIN OUT DIAGRAMS DESCRIBE THE FUNCTIONS OF THE PINS OF THE 8088 FOR MAXIMUM MODE AND MINIMUM MODE. (I.E. THE ADDRESS/DATA SIGNALS, THE STATUS SIGNALS, THE CONTROL SIGNALS, THE INTERRUPT SIGNALS, AND DMA SIGNALS)	X
1.3 GIVE THE MINIMUM-SYSTEM-MODE INTERFACE AND GIVE THE MAXIMUM-SYSTEM-MODE INTERFACE BY USING BLOCK CIRCUIT DIAGRAMS FOR THE COMPUTER SYSTEMS. (I.E. THE MAXIMUM MODE REQUIRES THE 8288 BUS CONTROLLER; AND MAY ALSO INCLUDE THE 8289 BUS ARBITER)	X
1.4 DESCRIBE HOW THE 8086/8088 MPU IS DIVIDED INTO THE BUS INTERFACE UNIT (BIU) AND EXECUTION UNIT (EU)	X
1.5 DESCRIBE HOW THE SYNCHRONIZATION FOR INTERNAL AND EXTERNAL OPERATIONS OF THE 8086/8088 IS ACHIEVED USING THE 8284 CLOCK GENERATOR. (I.E. THE SYSTEM CLOCK)	X
1.6 DEFINE THE BUS CYCLE USED TO ACCESS MEMORY, I/O DEVICES AND THE INTERRUPT CONTROLLER (PIC)	X
1.7 EXPLAIN THE DIFFERENCE BETWEEN 2ND AND 3RD GENERATION MPU'S BY REVIEWING THE "INSTRUCTION EXECUTION SEQUENCE" OF A SIMPLE PROGRAM	X
	CHAPTERS 2, 3, 4

COURSE NAME: CODE NO.:

INTERFACING CET 315 - 6

2.0 MEMORY INTERFACE OF THE 8086/8088

THE FOLLOWING SUPPORT CHIPS OF THE 8086/8088: BUS CONTROLLER, CLOCK GENERATOR, LATCHES, LINE DRIVERS, BUFFERS, TRANSCEIVERS, DECODERS, DYNAMIC REFRESHER, RAM, ROM, EPROM WILL BE STUDIED. THE REFERENCE TEXTS, SUPPLEMENTARY NOTES, ETC. MAY USE OR DESCRIBE DIFFERENTLY MANUFACTURED IC CHIPS, BUT THE PRINCIPLES ARE THE SAME.

UPON SUCCESSFUL COMPLETION OF THIS REVIEW AND AUGMENTATION UNIT, THE STUDENT WILL BE ABLE TO:

LEARNING ACTIVITIES	REQUIRED RESOURCES
2.1 GIVE THE MEMORY INTERFACE BLOCK DIAGRAM FOR EITHER THE MINIMUM-MODE-SYSTEM OR MAXIMUM-MODE-SYSTEM	TEXT
2.2 BRIEFLY DESCRIBE THE ADDRESS SPACE AND DATA ORGANIZATION	
2.3 DISTINGUISH BETWEEN THE READ BUS CYCLE AND THE WRITE BUS CYCLE	
2.4 DESCRIBE WHY DEMULTIPLEXING OF THE ADDRESS/DATA BUS IS NEEDED. AND ALSO, WHAT AND WHY THE LATCHES, BUFFERS, LINE DRIVERS ARE NEEDED.	
2.5 DISCUSS HOW ROM, PROM, EPROM DEVICES ARE INTERFACED TO THE 8086/8088. RELATE HOW THE EPROM DEVICES: 2708, 2716, 2732, 2764 ARE USED WITH THE 8086/8088	
2.6 DISCUSS HOW STATIC RAM DEVICES ARE INTERFACED TO THE 8086/8088 IN MINIMUM MODE AND MAXIMUM MODE	
2.7 DISCUSS HOW THE DYNAMIC RAM DEVICES ARE INTERFACED TO THE 8086/8088 IN MAXIMUM MODE. RELATE HOW THE DYNAMIC REFRESH CONTROLLER 8202 IS NEEDED ALONG WITH BUS CONTROLLER, LATCHES, TRANSCEIVERS, AND DECODER.	

CHAPTER 5

COURSE NAME: **CODE NO.:**

INTERFACING CET 315 - 6

3.0 MEMORY MAPPING FOR THE 8086/8088

UPON SUCCESSFUL COMPLETION OF THIS UNIT
THE STUDENT WILL BE ABLE TO:

LEARNING ACTIVITIES	REQUIRED RESOURCES
3.1 DESCRIBE THE DIFFERENCE BETWEEN LOGICAL ADDRESSING AND PHYSICAL ADDRESSING	TEXT & HANDOUTS
3.2 DESCRIBE THE DIFFERENCE BETWEEN MEMORY MAPPED VERSUS ISOLATED I/O ADDRESSING	TEXT & HANDOUTS
3.3 DESCRIBE WHAT THE INTERRUPT VECTOR TABLE IS USED FOR	HANDOUTS
3.4 UNDERSTAND WHY THE SYSTEM MEMORY MAP AND THE I/O SPACE MAP IS USED IN A MICROCOMPUTER DESIGN	HANDOUTS
3.5 WRITE PROGRAMS THAT INITIALIZE THE FOLLOWING SUPPORT CHIPS ADDRESS DECODED FOR EITHER A MEMORY MAP OR I/O MAP: PROGRAMMABLE PERIPHERAL INTERFACE (PPI) 8255; PROGRAMMABLE INTERRUPT CONTROLLER (PIC) 8259 PROGRAMMABLE INTERVAL TIMER (PIT) 8253	
3.6 USING THE REFERENCE DATA SHEET ON THE PPI, AND EARLIER SAMPLE PROGRAMS AS A GUIDE, BE ABLE TO WRITE A PROGRAM THAT WOULD SATISFY ANY NEW SYSTEM CONSTRAINTS GIVEN AND IMPLIED WITHIN A REASONABLE PERIOD OF TIME (APPROX 1 HOUR). FOR EXAMPLE, WRITE A PROGRAM THAT WOULD USE I/O MAPPED PPI #7 PORT C AND PORT B, MODE 0, ALL OUTPUTS; PORT A, MODE 0, ALL INPUT SIGNALS. CHECK IF D_0 & D_3 OF PORT A ARE 1'S IF AND ONLY IF THEN SEND OUT ON PORT B LINES D_0 - D_7 ALL 1'S.	
3.7 USING THE REFERENCE DATA SHEET ON THE PIC, AND EARLIER SAMPLE PROGRAMS AS A GUIDE, BE ABLE TO WRITE A PROGRAM THAT WOULD SATISFY ANY NEW SYSTEM CONSTRAINTS GIVEN AND IMPLIED WITHIN A REASONABLE PERIOD OF TIME (APPROX 1 HOUR). FOR EXAMPLE, WRITE A PROGRAM THAT WILL MASK OFF IR0 - IR3 IF AND ONLY IF ALL IR0 - IR3 ARE "INACTIVE".	

LEARNING ACTIVITIES	REQUIRED RESOURCES
3.8 USING THE REFERENCE DATA SHEET ON THE PIT, AND EARLIER SAMPLE PROGRAMS AS A GUIDE, BE ABLE TO WRITE A PROGRAM THAT WOULD SATISFY ANY NEW SYSTEM CONSTRAINTS GIVEN AND IMPLIED WITHIN A REASONABLE PERIOD OF TIME (APPROX 1 HOUR). FOR EXAMPLE, WRITE A PROGRAM THAT WILL GENERATE A "NOTE" USING THE PIT, MODE 3, I.E. SQUARE WAVE GENERATOR, WIRED TO THE PERMANENT MAGNET SPEAKER.	CHAPTER 5, 6

COURSE NAME: **CODE NO.:**

INTERFACING CET 315 - 6

4. INPUT/OUTPUT INTERFACE OF THE 8086/8088

THE FOLLOWING SUPPORT CHIPS OF THE 8086/8088: PROGRAMMABLE PERIPHERAL INTERFACE (PPI), BUS CONTROLLER, CLOCK GENERATOR, LATCHES, LINE DRIVERS, BUFFERS, TRANSCEIVERS, DECODERS WILL BE STUDIED. THE REFERENCE TEXTS, SUPPLEMENTARY NOTES, ETC. MAY USE OR DESCRIBE DIFFERENTLY MANUFACTURED IC CHIPS, BUT THE PRINCIPLES ARE THE SAME.

UPON SUCCESSFUL COMPLETION OF THIS UNIT,
THE STUDENT WILL BE ABLE TO:

LEARNING ACTIVITIES	REQUIRED RESOURCES
4.1 GIVE THE INPUT/OUTPUT INTERFACE BLOCK DIAGRAM FOR EITHER THE MINIMUM-MODE-SYSTEM OR MAXIMUM-MODE-SYSTEM	
4.2 BRIEFLY DESCRIBE THE ADDRESS SPACE AND DATA ORGANIZATION FOR INPUT/OUTPUT. (I.E. THE ISOLATED I/O MAP)	
4.3 USE THE IN AND OUT INSTRUCTIONS ON VARIOUS PORTS.	
4.4 DISTINGUISH BETWEEN THE INPUT BUS CYCLE AND THE OUTPUT BUS CYCLE	
4.5 IMPLEMENT A 64 BIT PARALLEL OUTPUT PORT USING 8 BYTE WIDE PORTS	
4.6 IMPLEMENT PARALLEL INPUT/OUTPUT (I/O) USING ISOLATED I/O MAPPED INTERFACE OF THE PROGRAMMABLE PERIPHERAL INTERFACE (PPI) TO THE MINIMUM MODE 8086 SYSTEM	
4.7 IMPLEMENT PARALLEL INPUT/OUTPUT (I/O) USING MEMORY MAPPED I/O INTERFACE OF THE PROGRAMMABLE PERIPHERAL INTERFACE (PPI) TO THE MINIMUM MODE 8086 SYSTEM	

CHAPTER 6

COURSE NAME: **CODE NO.:**

INTERFACING CET 315 - 6

5. INTERRUPT INTERFACE OF THE 8086/8088

THE FOLLOWING SUPPORT CHIPS OF THE 8086/8088: PROGRAMMABLE INTERRUPT CONTROLLER (PIC), BUS CONTROLLER, CLOCK GENERATOR, LATCHES, LINE DRIVERS, BUFFERS, TRANSCEIVERS, WILL BE STUDIED. THE REFERENCE TEXTS, SUPPLEMENTARY NOTES, ETC. MAY USE OR DESCRIBE DIFFERENTLY MANUFACTURED IC CHIPS, BUT THE PRINCIPLES ARE THE SAME.

UPON SUCCESSFUL COMPLETION OF THIS UNIT,
THE STUDENT WILL BE ABLE TO:

LEARNING ACTIVITIES	REQUIRED RESOURCES
5.1 GIVE THE 5 TYPES OF INTERRUPTS POSSIBLE AND THEIR PRIORITY. (I.E. EXTERNAL HARDWARE INTERRUPTS, SOFTWARE INTERRUPTS, INTERNAL INTERRUPTS, NONMASKABLE INTERRUPT, AND RESET INTERRUPT)	
5.2 USE THE 256 ENTRY INTERRUPT VECTOR TABLE AND THE INTERRUPT INSTRUCTIONS: (CLI, STI, INT n , INTO, HLT, AND WAIT)	
5.3 MASK OUT OR DISABLE INTERRUPTS OF EXTERNAL HARDWARE INTERRUPTS USING THE SOFTWARE INSTRUCTION CLI. ENABLE INTERRUPTS BY USING THE STI INSTRUCTION.	
5.4 GIVE THE BLOCK DIAGRAM FOR EXTERNAL HARDWARE INTERRUPT INTERFACES IN MINIMUM MODE 8086 SYSTEMS	
5.5 GIVE THE BLOCK DIAGRAM FOR EXTERNAL HARDWARE INTERRUPT INTERFACES IN MAXIMUM MODE 8086 SYSTEMS	
5.6 DETAIL THE EXTERNAL HARDWARE INTERRUPT SEQUENCE OF EVENTS. (I.E. INTERRUPT ACKNOWLEDGE BUS CYCLE)	
5.7 DETAIL THE INTERNAL ARCHITECTURE OF THE PROGRAMMABLE INTERRUPT CONTROLLER (PIC) USING BLOCK DIAGRAMS	
5.8 PROGRAM THE PROGRAMMABLE INTERRUPT CONTROLLER OR PIC BY INITIALIZING THE COMMAND WORDS (ICW), ACCESSING THE OPERATIONAL COMMAND WORDS (OCW)	
5.9 IMPLEMENT THE PIC IN A MASTER/SLAVE CONFIGURATION INTERRUPT INTERFACE FOR A MINIMUM MODE 8086 SYSTEM.	
5.10 IMPLEMENT THE PIC IN A MASTER/SLAVE CONFIGURATION INTERRUPT INTERFACE FOR A MAXIMUM MODE 8086 SYSTEM.	CH. 6

COURSE NAME: **CODE NO.:**

INTERFACING CET 315 - 6

6. CONSOLES, KEYBOARDS, DISK DRIVES

UPON SUCCESSFUL COMPLETION OF THIS UNIT, THE STUDENT WILL BE ABLE TO:

TEXT: 16 BIT MPU'S

LEARNING ACTIVITIES	REQUIRED RESOURCES
6.1 DESCRIBE THE HARDWARE ELEMENTS OF COMPUTER SYSTEM IN GENERAL TERMS (I.E. INPUTS, OUTPUTS, MEMORY, CPU)	CHAPTER 1
6.2 DESCRIBE THE NATURE OF THE CENTRONICS PARALLEL INTERFACE	TEXT & CHAPTER 9 "DAILEY"
6.3 DISCUSS DATA COMMUNICATIONS AND NETWORKING TERMINOLOGY: DATA CODES, PARALLEL AND SERIAL TRANSMISSION, BAUD RATE, MODULATION AND DEMODULATION, MODEMS, DCE-DTE INTERFACE, DATA COMMUNICATIONS STANDARDS: IEEE-488 GPIB, ETHERNET, RS-449	HANDOUTS & CHAPTER 9 "DAILEY"
6.4 DESCRIBE THE VARIOUS TECHNIQUES OF A/D AND D/A CONVERSION.	CHAPTER 7 "DAILEY"
6.5 IMPLEMENT A/D AND D/A USING POLLED, DMA AND INTERRUPT MODES. USING THE MAT TRAINERS EQUIPED WITH: SERVOMOTORS, SPEAKERS, MICROPHONES	HANDOUTS
6.6 DISCUSS THE PRINCIPLE OF OPERATION OF THE VARIOUS CONSOLE SCREENS: RASTER SCAN CRT, COMPOSITE VIDEO, AND RGB MONITORS.	CHAPTER 1, 8
6.7 DISCUSS THE PRINCIPLES INVOLVED IN THE OPERATION OF THE KEYBOARDS: SWITCH MATRIX, SCANNING AND ENCODING, SWITCH DEBOUNCING.	CHAPTER 8
6.8 DISCUSS THE DISK DRIVE SUBSYSTEM OF MICRO-COMPUTER SYSTEMS AS TO: DIGITAL DATA ENCODING TECHNIQUES, FLOPPY DISK CONTROLLER CHIP 8272 OPERATION, AND DISK CARE.	CHAPTER 7

COURSE NAME: **CODE NO.:**

INTERFACING CET 315 - 6

7. REGISTERS, ADDRESSING MODES, AND INSTRUCTION SET OF THE 68000

UPON SUCCESSFUL COMPLETION OF THIS UNIT, THE STUDENT WILL BE ABLE TO:

2ND TEXT:

LEARNING ACTIVITIES	REQUIRED RESOURCES
7.1 UNDERSTAND THE ARCHITECTURE OF THE 68000 MPU BY DESCRIBING ITS: REGISTERS, ADDRESSING MODES, AND INSTRUCTION SET.	
7.2 DESCRIBE USING BLOCK DIAGRAMS THE INTERFACE SIGNALS FOR THE 68000: ADDRESS BUS, DATA BUS, ASYNCHRONOUS BUS CONTROL, BUS ARBITRATION CONTROL, INTERRUPT CONTROL, SYSTEM CONTROL, PERIPHERAL CONTROL (OR SYNCH. CONTROL, AND PROCESSOR STATUS.	
7.3 DESCRIBE INTERNAL EXECUTION CONTROL ARCHITECTURE: INSTRUCTION REGISTER, INSTRUCTION DECODER, CONTROL UNIT, EXECUTION UNIT.	CHAPTER 1,2,3,4
7.4 DEMONSTRATE HOW TO USE MS DOS AND THE TED EDITOR TO LOAD AND WRITE SIMPLE 68000 ASSEMBLY PROGRAMS ON THE IBM PC, THEN USE THE CROSS ASSEMBLER, THEN DOWNLOAD OR INTERFACE TO THE 68000 URDA KITS).	
7.5 TRANSFER 68000 HEX CODE PROGRAMS (FIRST WRITTEN USING THE TED EDITOR ON THE IBM PC) OVER TO THE URDA KIT 68000. RUN THE PROGRAMS ON THE URDA KITS: FLASH, SIREN, NAME	HANDOUTS

COURSE NAME: **CODE NO.:**

INTERFACING CET 315 - 6

8. ASYNCHRONOUS MEMORY AND I/O INTERFACE OF THE 68000

UPON SUCCESSFUL COMPLETION OF THIS UNIT, THE STUDENT WILL BE ABLE TO: TEXT

LEARNING ACTIVITIES REQUIRED RESOURCES

8.1 PRODUCE A BLOCK DIAGRAM FOR THE ASYNCHRONOUS MEMORY AND I/O INTERFACE

8.2 DETAIL THE ADDRESS SPACE AND DATA ORGANIZATION OF THE 8M WORD ADDRESSES, OR 16M BYTE ADDRESSES.

8.3 PRODUCE THE SIMPLE MEMORY MAP FOR THE 68000, INDICATING: EXCEPTION VECTOR TABLE, AND GENERAL USE MEMORY.

8.4 USING FUNCTION CODES PARTITION THE MEMORY SUBSYSTEM HARDWARE INTO: USER PROGRAM SEGMENT, USER DATA SEGMENT, SUPERVISOR PROGRAM SEGMENT, AND SUPERVISOR DATA SEGMENT.

8.5 DISCUSS THE READ MEMORY AND I/O CYCLE TIMING

8.6 DISCUSS THE WRITE MEMORY AND I/O CYCLE TIMING

8.7 WRITE PROGRAMS EMPLOYING THE: USER STACK, AND SUPERVISOR STACK.

8.8 UNDERSTAND THE DYNAMIC RAM MEMORY (SOFTWARE-REFRESHED 64K BYTE) SUBSYSTEM BLOCK DIAGRAM

8.9 DISCUSS THE 8 BIT PERIPHERAL INTERFACE ADAPTER, (6821 OR PIA), USING BLOCK DIAGRAMS. USE THE MOVEP INSTRUCTION WITH THE PIA TO TRANSFER DATA EXTERNALLY.

8.10 DISCUSS HOW TWO PIA'S CAN BE USED TO TRANSFER DATA IN PARALLEL PRODUCING 16 BIT PORTS

8.11 PROGRAM THE 16 BIT PARALLEL INTERFACE /TIMER 68230 (PI/T) CHIP UNDER THE FOUR MODES.

8.12 PROGRAM THE ASYBCHRONOUS COMMUNICATIONS INTERFACE ADAPTER 6850 (ACIA) CHIP FOR SERIAL DATA TRANSFER

8.13 INTERPRET THE SCHEMATIC DIAGRAMS USING THE RS-232C STANDRAD, MODEMS, DCE, DTE EQUIPMENT, AND THE INTERFACE MODEM CHIP 68HC51 CHAPTER 8

COURSE NAME: CODE NO.:

INTERFACING CET 315 - 6

9. SYNCHRONOUS MEMORY AND I/O INTERFACE OF THE 68000

UPON SUCCESSFUL COMPLETION OF THIS UNIT, THE STUDENT WILL BE ABLE TO:

TEXT: 16 BIT MPU'S

LEARNING ACTIVITIES	REQUIRED RESOURCES
9.1 PRODUCE THE SYNCHRONOUS MEMORY AND I/O INTERFACE PIN OUT DIAGRAM.	
9.2 DISCUSS THE SYNCHRONOUS BUS CYCLE TIMING	
9.3 SHOW HOW TO USE A CONVERSION CIRCUIT TO INTERFACE THE 6821 PIA TO THE SYNCHRONOUS INTERFACE BUS.	
9.4 WRITE A PROGRAM THAT CONTROLS THE PIA CHIPS SUCH THAT 8, 16, AND 32 BIT PARALLEL PORTS ARE POSSIBLE FOR INPUT OR OUTPUT SIGNALS.	CHAPTER 7

COURSE NAME: CODE NO.:

INTERFACING CET 315 - 6

10. EXCEPTION PROCESSING OF THE 68000

UPON SUCCESSFUL COMPLETION OF THIS UNIT, THE STUDENT WILL BE ABLE TO:

TEXT: 16 BIT MPU'S

LEARNING ACTIVITIES	REQUIRED RESOURCES
10.1 KNOW THE VARIOUS EXCEPTIONS: EXTERNAL EXCEPTION FUNCTIONS, HARDWARE RESET, AND USER DEFINED EXTERNAL INTERRUPTS.	
10.2 USE THE EXCEPTION VECTOR TABLE TO DISCOVER WHAT TYPE OF ERROR OR EVENT CAUSED THE INTERRUPT.	
10.3 KNOW THE VARIOUS PRIORITIES OF EXCEPTIONS: RESET, BUS ERROR, ADDRESS ERROR ARE GROUP 0 (HIGHEST) TRACE, INTERRUPT, ILLEGAL, PRIVILEGE ARE GROUP 1 TRAP, TRAPV, CHK, ZERO DIVIDE ARE GROUP 2 (LOWEST)	
10.4 PRODUCE A BLOCK DIAGRAM OF THE GENERAL INTERRUPT INTERFACE. (I.E. UP TO 192 DEVICES PERMITTED).	
10.5 KNOW HOW TO ASSIGN ONE OF THE 7 PRIORITY LEVELS FOR AN EXTERNAL HARDWARE DEVICE INTERRUPT, AND HOW TO USE THE INTERRUPT MASK.	
10.6 DETAIL THE GENERAL INTERRUPT PROCESSING SEQUENCE OF EVENTS	
10.7 PRODUCE THE TYPICAL GENERAL INTERRUPT INTERFACE CIRCUIT	
10.8 PRODUCE A BLOCK DIAGRAM OF THE AUTOVECTOR INTERRUPT INTERFACE. (I.E. ONLY UP TO 7 DEVICES PERMITTED).	
10.9 PRODUCE A TYPICAL AUTOVECTOR INTERRUPT INTERFACE CIRCUIT	
10.10 KNOW HOW TO USE THE EXCEPTION INSTRUCTIONS FOR: BUS ERROR, RESET EXCEPTION, AND INTERNAL EXCEPTION FUNCTIONS.	CHAPTER 6

V. METHOD(S) OF EVALUATION

1.

THE STUDENT WILL BE ASSESSED THROUGH A SERIES OF THREE (3) WRITTEN TESTS. THESE TESTS WILL EACH BE WEIGHTED TO 20% OF THE FINAL MARK.

THE TENTATIVE DATES ARE: OCT 5 /91
NOV 3 /91
DEC 19/91

THESE TEST DATES WILL BE RE-ANNOUNCED APPROXIMATELY ONE WEEK IN ADVANCE.

2.

THE STUDENT WILL BE ASSESSED THROUGH A SERIES OF UNANNOUNCED QUIZZES. THE TOTAL WEIGHT OF THESE QUIZZES ARE NOT TO EXCEED 10% OF THE FINAL MARK.

3.

THE STUDENT WILL BE ASSESSED THROUGH A SERIES OF LAB ASSIGNMENTS. COLLECTIVELY THESE ASSIGNMENTS WILL BE WEIGHTED TO 25% OF THE FINAL MARK.

4.

THE STUDENT WILL BE ASSESSED ON HIS/HER ABILITY TO ANSWER QUESTIONS ABOUT THE LAB ASSIGNMENT ONCE SUBMITTED. THE STUDENT'S RESPONSE TO THESE LAB DEMONSTRATION QUESTIONS WILL BECOME PART OF HER/HIS "PRACTICAL DEMONSTRATION" MARK. THIS MARK WILL BE WEIGHTED TO 5% OF THE FINAL MARK.

5.

THE STUDENT ATTENDING MORE THAN 80% OF THE TIME WILL RECEIVE A BONUS OF 2%.

COURSE NAME: **CODE NO.:**

INTERFACING CET 205 - 5

SUMMARY OF FINAL MARK

1.	TESTS	60%
2.	QUIZZES	10%
3.	ASSIGNMENTS	25%
4.	DEMOS	5%
		100%
5.	ATTENDANCE	2% BONUS ONLY

COURSE GRADING SCHEME

A+	90+	OUTSTANDING ACHIEVEMENT
A	80 - 89	ABOVE AVERAGE ACHIEVEMENT
B	70 - 79	AVERAGE ACHIEVEMENT
C	55 - 69	SATISFACTORY ACHIEVEMENT
U		UNSATISFACTORY GIVEN AT MIDTERM ONLY
S		SATISFACTORY GIVEN AT MIDTERM ONLY
R		REPEAT
X		A TEMPORARY GRADE THAT IS LIMITED TO INSTANCES WHERE SPECIAL CIRCUMSTANCES HAVE PREVENTED THE STUDENT FROM COMPLETING OBJECTIVES BY THE END OF THE SEMESTER. AN "X" GRADE MUST HAVE THE DEAN'S APPROVAL AND HAS A MAXIMUM TIME LIMIT OF 120 DAYS.

COURSE NAME: **CODE NO.:**

INTERFACING CET 315 - 6

3. UPGRADING OF INCOMPLETES

WHEN A STUDENT'S COURSE WORK IS INCOMPLETE OR FINAL GRADE IS BELOW 55%, THERE IS THE POSSIBILITY OF UPGRADING TO A PASS WHEN THE STUDENT'S PERFORMANCE WARRANTS IT. ATTENDANCE AND ASSIGNMENT COMPLETION WILL HAVE A BEARING ON WHETHER UPGRADING WILL BE ALLOWED. A "REPEAT" GRADE ON ALL TESTS WILL REMOVE THE OPTION OF ANY UPGRADING AND AN "R" GRADE WILL RESULT. THE HIGHEST ON A RE-WRITTEN TEST OR ASSIGNMENT WILL BE 56%.

THE METHOD OF UPGRADING IS AT THE DISCRETION OF THE TEACHER AND MAY CONSIST OF ONE OR MORE OF THE FOLLOWING OPTIONS:

ASSIGNED MAKE-UP WORK
RE-DOING PROJECTS
RE-DOING OF TESTS
WRITING OF COMPREHENSIVE SUPPLEMENTAL EXAMINATION

COURSE NAME: CODE NO.:

INTERFACING CET 315 - 6

VI. REQUIRED STUDENT RESOURCES

THE TEXT REQUIRED TO BE PURCHASED BY STUDENTS ARE:

1.

W/90 CET 228 COURSE TEXT

8088/80886 MPU TEXT (1ST TEXT FOR THIS COURSE)

"MICROCOMPUTER SERVICING, PRACTICAL SYSTEMS AND TROUBLESHOOTING"
BY STUART M. ASSER, VINCENT I\J. STIGLIANO, RICHARD F. BAHRENBURG
MERRILL PUBLISHING, 1990

2.

68000 MPU TEXT (2ND TEXT FOR THIS COURSE)

"THE M68000 MICRIPROCESSOR FAMILY"
BY YU-CHENG LIU
PUBLISHER: PRENTICE-HALL, 1991

3.

SUPPLEMENTARY NOTES FOR CET 315

PREPARED BY PETER SAVICH

4.

THE STUDENTS WILL ALSO BE EXPECTED TO PURCHASE APPROXIMATELY 10 FLOPPY DISKS 5 AND ONE QUARTER INCH, DOUBLE SIDED, DOUBLE DENSITY.

VII. ADDITIONAL RESOURCE MATERIALS (AVAILABLE IN COLLEGE LIBRARY)

THERE ARE MANY OTHER BOOKS ON ASSEMBLER LANGUAGE FOR THE 8086/8088 MICROPROCESSOR FAMILY:

1.

F/90 COURSE FOR CET 315

16 BIT ARCHITECTURES
BY AVTAR SINGH AND WALTER TRIEBEL
PUBLISHER: PRENTICE-HALL

2.

W/89 COURSE TEXT FOR CET 228

SMALL COMPUTER THEORY AND APPLICATIONS
BY DENTON DAILEY
PUBLISHER: MCGRAW HILL

3.

F/88 COURSE TEXT FOR CET 205

ADVANCED MICROPROCESSORS, BY HEATHKIT EDUCATIONAL SYSTEMS
THERE ARE 3 BOOKS: BOOK I, BOOK II , AND STUDENT WORKBOOK.

THERE ARE MANY OTHER BOOKS ON ASSEMBLER LANGUAGE FOR THE 68000 MICROPROCESSOR FAMILY:

M68000 PROGRAMMER'S REFERENCE MANUAL
PUBLISHED BY MOTOROLA

VIDEO TAPES: COMPAQ CAD/CAE

PERIODICALS: PC MAG, BYTE MAG, COMPUTING CANADA

Most of the irrelevant material

COURSE NAME: **CODE NO.:**

INTERFACING CET 315 - 6

VIII. SPECIAL NOTES

FOR THE ELECTRICAL & ELECTRONIC STUDENTS THE CET315 COURSE IS BEING OFFERED THIS YEAR (1990) AND FOR THE FUTURE, USING THE 8086/8088 MICROPROCESSOR AND THE 68000. FOR ANY REPEATING STUDENTS OR STUDENTS WITH PAST CREDIT IN CET315, THE COURSE WAS OFFERED BEFORE USING THE 6800, LSI-11, AND 8088 MICROPROCESSORS. THE COLLEGE HAS UPGRADED TO THE MORE POWERFUL 8086/8088 FAMILY AND 68000 FAMILY OF MICROPROCESSOR MICROCOMPUTER SYSTEMS.

THE CET306 "PDP-11" COURSE OF THE SIXTH SEMESTER COMPLETES ALL THE COMPUTER RELATED COURSE MATERIAL OF THE ELECTRICAL/ ELECTRONIC PROGRAM. THUS THE 8088 MICROPROCESSOR, AND 8088 ASSEMBLER LANGUAGE OF THE IBM PC MICROCOMPUTER IS WELL STUDIED. THREE COURSES: CET205, CET228, AND CET315 DETAIL THIS 8086/8088 FAMILY. THE 68000 FAMILY OF MICROPROCESSORS STUDIED IN CET315 IS VERY POPULAR AND COMPUTER SYSTEMS SUCH AS THE AMIGA, MACINTOSH USE THIS MPU.

THE INTENTION OF ALL THIS MICROPROCESSOR TECHNOLOGY STUDIES IS TO GAIN ENOUGH MPU INTERFACING KNOWLEDGE TO INCORPORATE THE PROPER MPU FAMILY INTO THE STUDENT'S ELECTRICAL OR ELECTRONIC THIRD YEAR "RESEARCH PROJECT(S)".

INSTRUCTORS (PROFESSORS) RESERVE THE RIGHT TO MAKE CHANGES TO THE COURSE OUTLINES WHERE NECESSARY.

VIII. SPECIAL NOTES

SAFETY GUIDELINES TO USE WHILE WORKING WITH ELECTRONICS AND COMPUTER SYSTEMS

ALWAYS WORK IN A SAFE WORKING ENVIRONMENT. THIS SAFE ENVIRONMENT SHOULD BECOME A HABIT. THIS HABIT WILL ALLOW YOU TO LIVE, ENJOY LIFE LONGER.

ELECTRONIC EQUIPMENT IS FILLED WITH OPPORTUNITIES FOR ACCIDENTS. ELECTRIC SHOCK, BURNS FROM HOT METALS, CHIPS, ETC. ARE POSSIBLE IF NOT PRACTISING SAFE WORK HABITS.

LETHAL CURRENT CHART

AMPERES	EXPECTED OUTCOME
1.00	
0.80	
0.60	SEVERE BURNS
0.40	
0.20	DEATH
0.10	DEATH
0.09	EXTREME BREATHING DIFFICULTIES
0.08	BREATHING UPSET
0.07	LABOURED BREATHING
0.06	SEVERE SHOCK
0.05	MUSCULAR PARALYSIS
0.04	CAN NOT LET GO
0.03	VERY PAINFUL
0.02	PAINFUL
0.01	MILD SENSATION
0.001	THRESHOLD OF SENSATION

NOT PAYING ATTENTION TO DESIGN DRAWINGS, OR INCORRECTLY WIRING COMPONENTS MAY ACTUALLY CAUSE A DEVICE, CHIP TO EXPLODE. YOU MUST PROTECT YOURSELF FROM POSSIBLE EYE INJURY OR OTHER PHYSICAL HARM.

COURSE NAME: **CODE NO.:**

INTERFACING CET 315 - 6

THE FOLLOWING STEPS ARE A PART OF SAFE WORK HABITS, FOLLOWING THEM WILL REDUCE THE RISK OF ACCIDENT AND INJURY TO AN ACCEPTABLE LEVEL. THE PRECAUTIONS INVOLVED WILL MINIMIZE THE DAMAGE IF AN ACCIDENT DOES OCCUR. YOU MUST CONSTANTLY BE AWARE OF THE POTENTIAL HAZARDS AND PERIODICALLY CHECK YOUR SAFETY PRECAUTIONS.

1.
AVOID WORKING ON ENERGIZED EQUIPMENT IF AT ALL POSSIBLE. IN MANY CASES YOU CAN CONNECT TEST LEADS WITH THE POWER OFF AND THEN TURN ON THE POWER.

2.
JEWELRY SUCH AS RINGS, WATCHES, AND BRACELETS SHOULD NEVER BE WORN IN THE WORKPLACE. NOT ONLY ARE MOST OF THESE OBJECTS CONDUCTIVE, WHICH WILL CAUSE A SHOCK IF THEY CONTACT BOTH YOU AND THE ENERGIZED CIRCUIT, BUT THERE IS ALSO THE DANGER OF THEM CATCHING ON COMPONENTS OR ANY MOVING ELECTROMECHANICAL DEVICES.

3.
MAKE A PRACTICE OF ALWAYS STANDING ON A RUBBER MAT WHILE WORKING WITH ELECTRICITY. RUBBER MATS INSULATE YOU FROM THE FLOOR, WHICH IS USUALLY AT GROUND POTENTIAL. THIS REDUCES THE CHANCE OF AN ELECTRICAL PATH THROUGH YOUR BODY.

4.
ALWAYS BE AWARE OF POSSIBLE ELECTRICAL PATHS THROUGH YOUR BODY. IN MANY INSTANCES IT IS DESIRABLE TO REST PART OF YOUR HAND ON THE CHASSIS WHILE SUPPORTING A TEST PROBE. THIS WAY IF THERE IS A SHOCK, IT WILL GO THROUGH YOUR HAND, AND NOT THROUGH YOUR HEART.

5.

IF YOU MUST WORK ON ENERGIZED EQUIPMENT, USE ONLY ONE HAND AT A TIME. THIS PREVENTS A CURRENT FROM PASSING FROM ONE HAND, THROUGH YOUR BODY TO THE OTHER HAND.

6.
COMPONENTS SUCH AS TRANSISTORS OR RESISTORS MAY BECOME VERY HOT. THEY SHOULD NOT BE TOUCHED WITH BARE HANDS EVEN AFTER THE POWER HAS BEEN TURNED OFF.

7.
NEVER ROUTE CONNECTING WIRES OR TEST LEADS OVER TRANSISTORS OR LARGE RESISTORS. BECAUSE THEY GET HOT, THESE COMPONENTS CAN MELT THE WIRE COATING AND POSSIBLY SHORT CIRCUIT.

8.
NEVER ASSUME THAT JUST BECAUSE THE EQUIPMENT IS UNPLUGGED, IT IS SAFE. CAPACITORS CAN STORE EXTREMELY HIGH VOLTAGES. FOR EXAMPLE, THE CRT SCREEN FLYBACK TRANSFORMER. TO PROTECT YOURSELF, USE A GROUND STRAP TO SHORT THE COMPONENT'S LEADS TO GROUND BEFORE YOU PUT YOUR HAND CLOSE TO THEM, OR ATTACH A TEST LEAD. YOU MAY EVEN WANT TO LEAVE THE GROUND LEAD IN PLACE UNTIL YOU ARE THROUGH WORKING IN THAT AREA. THIS WILL PREVENT SHOCK EVEN IF YOU DO ACCIDENTLY TOUCH THE COMPONENT'S LEADS. BUT REMEMBER, USE A GROUNDED STRAP ONLY IF THE EQUIPMENT IS UNPLUGGED. REMOVE THE GROUND STRAP WHEN TESTING IS COMPLETED.

9.

TEST EQUIPMENT SHOULD ALWAYS BE PLUGGED INTO THE SAME OUTLET AS THE COMPUTER AND PERIPHERALS BEING USED. IF NOT, THERE IS A DANGER OF CONNECTING TO OPPOSITE PHASES OF THE POWER LINE. THIS WOULD RESULT IN A 220 VOLT DIFFERENCE IN THEIR POWER CONNECTIONS. ALTHOUGH THIS IS NOT NORMALLY A PROBLEM, THIS VOLTAGE COULD SHOW UP IF THERE IS ANOTHER FAILURE.

10.
NEVER WORK ON HIGH VOLTAGE EQUIPMENT ALONE. PRACTICE THE BUDDY SYSTEM. IF YOU SHOULD BECOME DISABLED YOUR BUDDY CAN TURN OFF THE POWER AND PROVIDE AID. A SEVERE SHOCK COULD MAKE YOU INCAPABLE OF DISENGAGING YOURSELF FROM THE EQUIPMENT. ALWAYS USE INSULATED TOOLS TO REDUCE THE POSSIBILITY OF SHOCK WHEN ADJUSTING A LIVE CIRCUIT.

11.
IT IS ALSO GOOD PRACTICE TO ALWAYS WEAR SAFETY GLASSES WHEN WORKING ON ELECTRONIC EQUIPMENT OR OPERATING POWER TOOLS OF ANY TYPE.